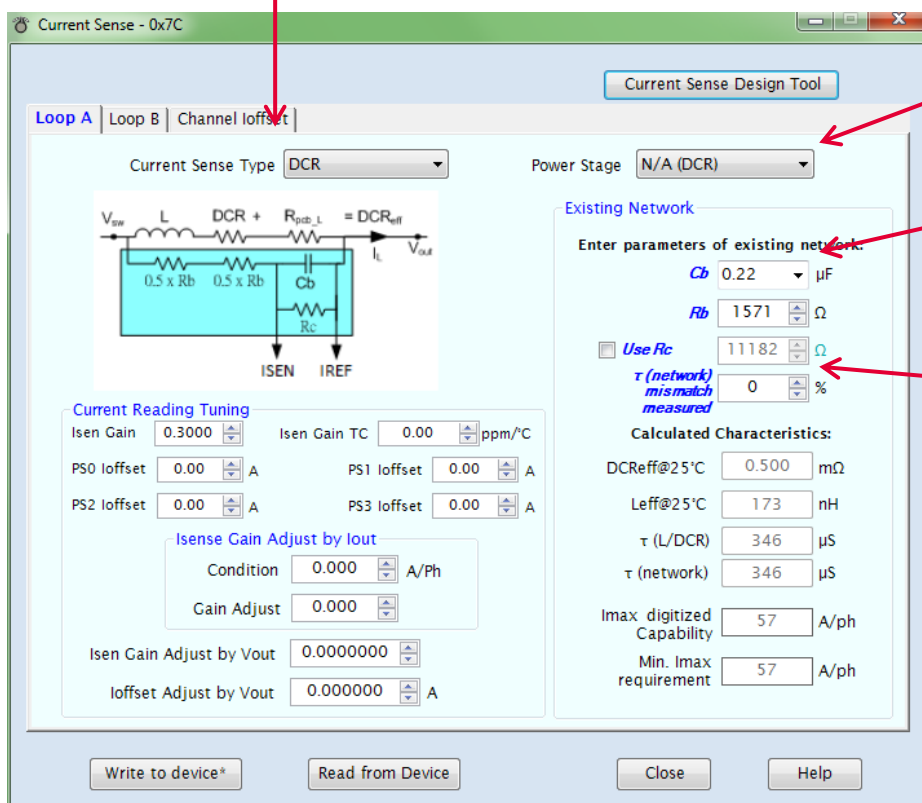


# Current sense... DCRsense

**Current Sense Type:** can be selected between DCR sense (as shown), DCR Shunt or Non-DCR ( i.e. Powerstage with internal current sense).

The graphical figure will change to match selection made. Here DCR sense is shown.



**Power stage.** When Current sense Type is selected to be Non-DCR then the family of powerstage used can be selected here. In this example grayed out and not selectable as DCRsense is selected.

**Cb and Rb:** Enter the real values used on the PCB for capacitor and resistor

**T ( Network) mismatch measured:** This is the mismatch in the two time constants  $R_b \cdot C_b$  and  $L/DCR$  for the real components. Explanation follows on next 2 pages

# Current sense... Current sense design tool

A tool to help calculate current sense parameters. Use knowledge from the 3 following theory slides to find suitable numbers to enter.

**First** enter some basic numbers for the design

**2nd step.** Enter Data for inductor used  
And the Cb capacitor 0.22uF  
recommended. T marging typical 2%

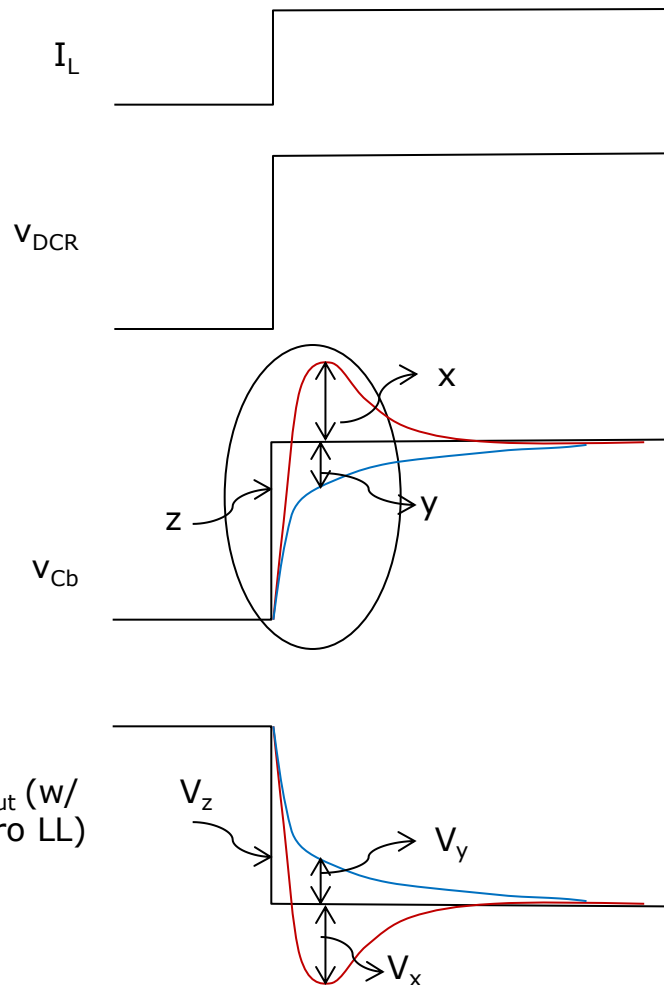
**3rd step.** Enter Data for Rb resistor

**Use Rc.** If there is a high DCR value the sense voltage may be needed to be divided down by using resistor Rc. If this is used mark the box and enter a number in the **Rc** field

**Isense gain.** Calculated value that can be used as Isense gain in the current sense window. It is to be used as starting point as final gain is determined by testing.

# Current sense... dynamic response: $R_b * C_b$ time constant

$$v_{Cb_x} = v_{DCR_x} * \frac{L / DCR}{R_b * C_b}, \quad s \rightarrow \infty$$



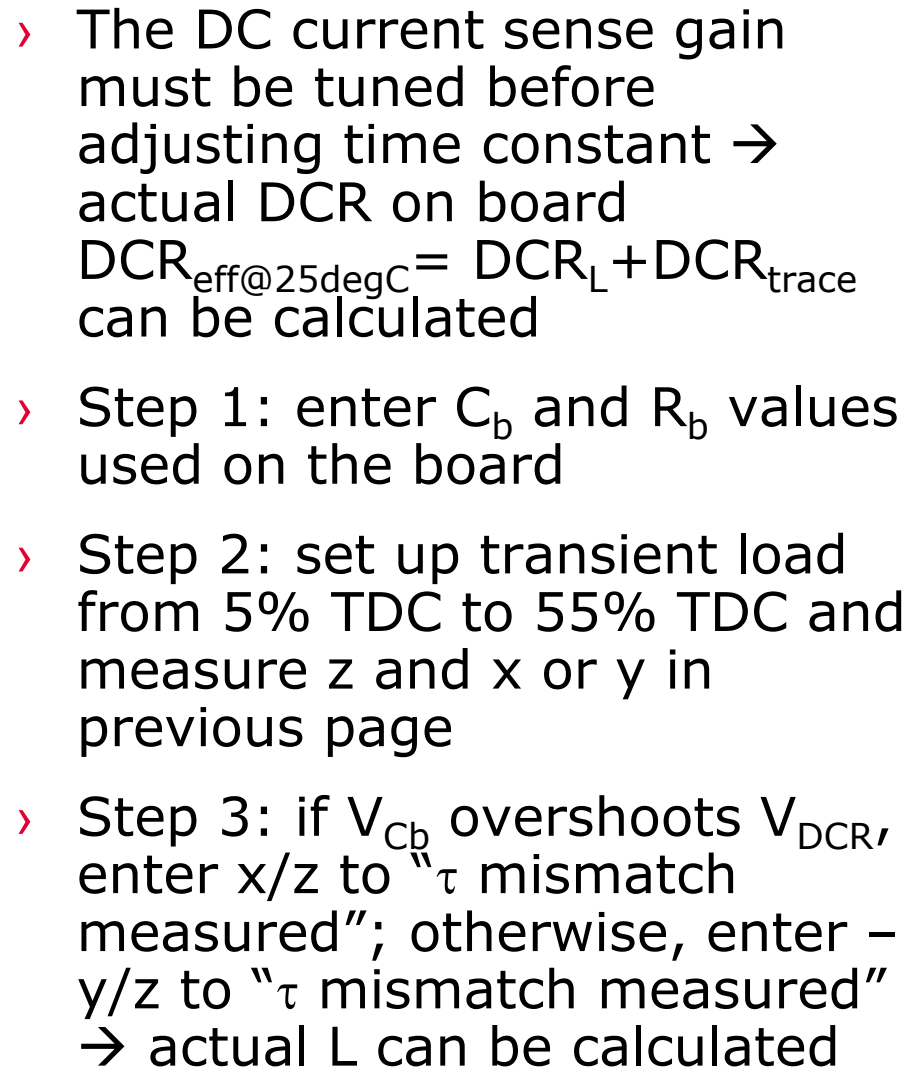
› Impact of how  $R_b * C_b$  compared to  $L / DCR_{eff}$ :

- If  $R_b * C_b = L / DCR_{eff}$ ,  $v_{Cb}$  will be the same  $v_{DCR}$  at any frequency
- If  $R_b * C_b < L / DCR_{eff}$ ,  $v_{Cb}$  will underdamp  $v_{DCR}$  which leads to overshoot/undershoot during transient when LL is non-zero. To adjust time constant:

- $(R_b * C_b)_{new} = (R_b * C_b)_{orig} * (1 + x/z)$

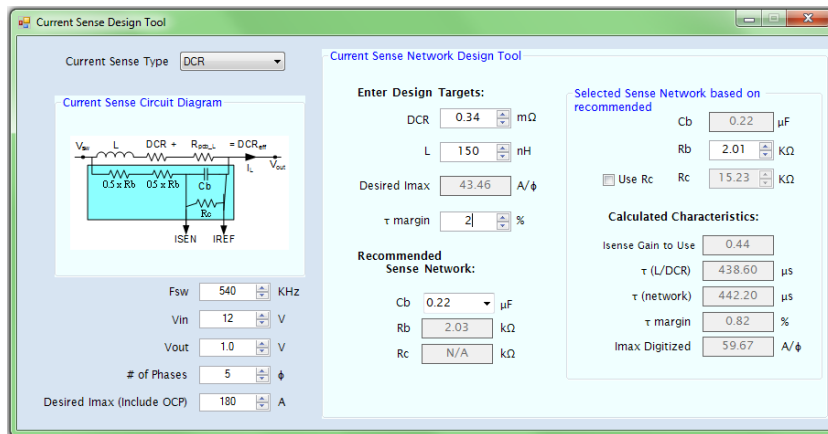
- If  $R_b * C_b > L / DCR$ ,  $v_{Cb}$  will overdamp  $v_{DCR}$ . To adjust time constant:

- $(R_b * C_b)_{new} = (R_b * C_b)_{orig} * (1 - y/z)$



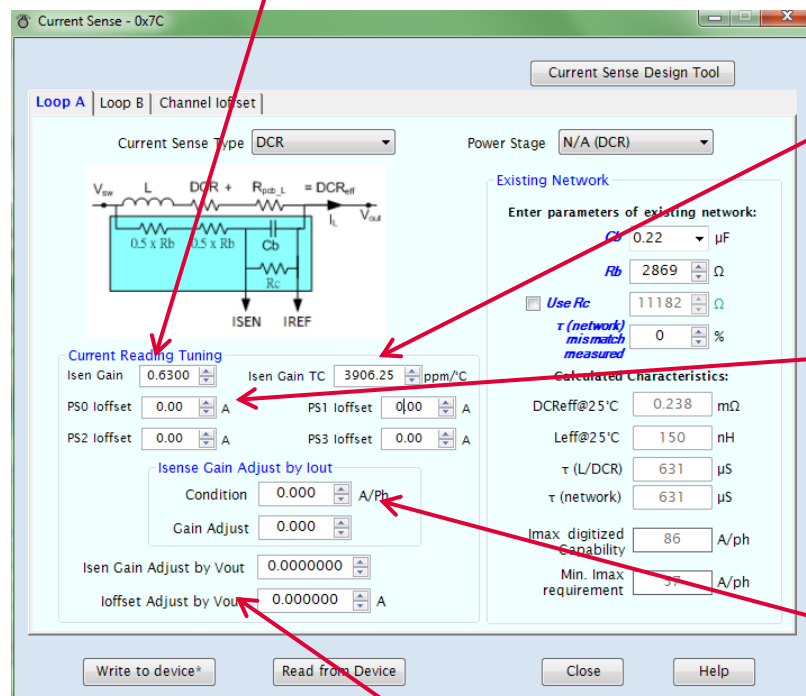
# Current sense... Adjust DCR sense network time constant – method 1: using transient waveforms with non-zero LL slope (2 of 2)

- › Step 5: Select the desired  $C_b$  value and then  $R_b$  will be calculated automatically
  - Tip: recommend to keep the same  $C_b$  value and only adjust  $R_b$  value to minimize modifications on board
- › Step 7: change the  $R_b$  or  $C_b$  to the new values on the board and verify DC current reading and time constants matching again
  - Iteration of DC current reading and time constant adjustments might be necessary



# Current sense... DCRsense

**Isen Gain.** The gain factor for the measured voltage across  $C_b$  that represent the current through the Inductor. Tuning this value such that the current reading gain is accurate from 0A to 2/3 of TDC with Isen gain TC set at 3906.25ppm/degC when temp change in inductor is small.  
To get a starting value set the gain=0.15mV/DCR



**Isen Gain TC** (Temperature Coefficient) This setting value is between 2000 ~ 4000 ppm/degC typically. Use the ideal copper TC=3906.25 first and then based on temperature compensation result of inductor DCR to trim this value. This value could be different by layout.

**PS0 Ioffset.** Adjustment of reported current for different PowerStates.  
As they may use different number of phases the reported current may change and can be compensated by adding an offset.

## Isense Gain Adjust by Iout

- Applies an optional gain adjustment to the current sense based on Iout
- For load currents greater than the specified A/ph Condition, the specified **Gain Adjust** value will be applied
- Recommended setting for **Current Sense Type=nonDCR** is 16A/ph

$$Isen\ Gain\ @\ I_x\ per\ phase = Isen\ Gain * (I_x - I_{condition}) * (1 + GainAdjust)$$

## Isense Gain Adjust by Vout

To allow for output voltage dependent changes in reported current.

# Current sense... Sense resistor

Current Sense - 0x7C

Current Sense Design Tool

Loop A | Loop B | Channel | Offset

Current Sense Type: DCR

Power Stage: N/A (Sense Resistor)

Existing Network

Enter parameters of existing network:

$R_b$  1  $\Omega$

☒ Use  $R_c R_b$  1  $\Omega$

Calculated Characteristics:

Reff@25°C 0.495 m $\Omega$

Imax digitized Capability 78 A/ph

Min. Imax requirement 59 A/ph

Current Reading Tuning

Isen Gain 0.3906 Isen Gain TC 0.00 ppm/°C

PS0 Ioffset 0.000 A PS1 Ioffset 0.000 A

PS2 Ioffset 0.000 A PS3 Ioffset 0.000 A

Isense Gain Adjust by Iout

Condition 0.000 A/ph

Gain Adjust 0.000

Isen Gain Adjust by Vout 0.0000000

Ioffset Adjust by Vout 0.000000 A

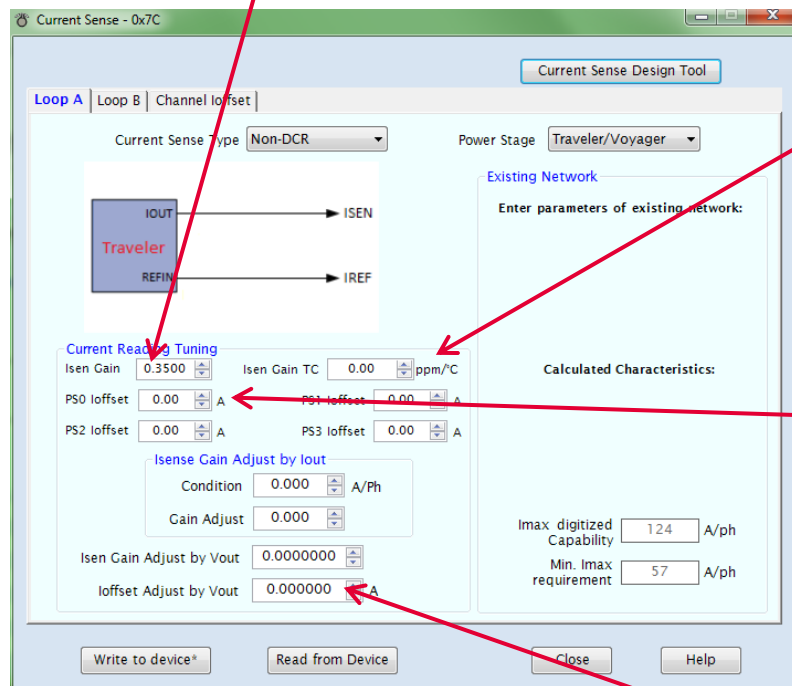
Write to device Read from Device Close Help

With a sense resistor instead of DCR sense most settings are similar.

# Current sense... Non-DCR

**Isen Gain.** Gain to use for the signal from the powerstage

To get a starting value set the gain=0.35 when using a powerstage like TDA21460



**Isen Gain TC.**

If needed Temperature Coefficient for Gain can be added. Typically set to 0

**PS0 Ioffset.** Adjustment of reported current for different PowerStates. As they may use different number of phases the reported current may change and can be compensated by adding an offset.

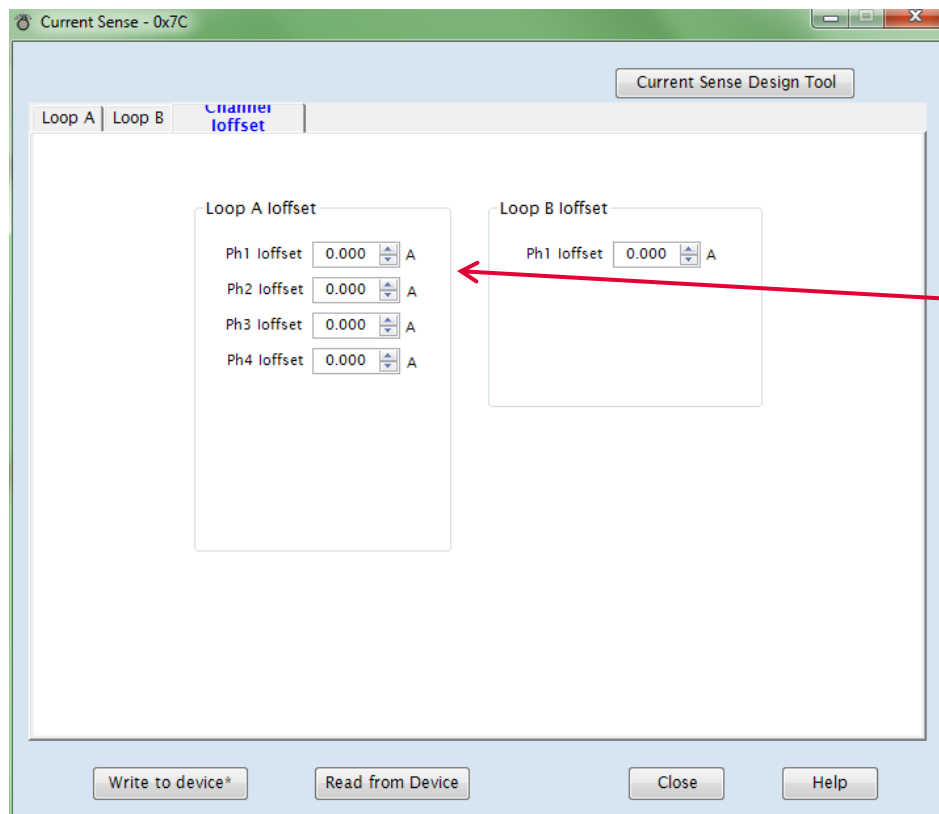
## Isense Gain Adjust by Iout

- Applies an optional gain adjustment to the current sense based on Iout
- For load currents greater than the specified A/ph Condition, the specified **Gain Adjust** value will be applied
- Recommended setting for *Integrated Current Sense Type (A)* is 16A/ph

$$\text{Isen Gain @ } I_x \text{ per phase} = \text{Isen Gain} * (I_x - I_{\text{condition}}) * (1 + \text{GainAdjust})$$



# Current sense... Offset



**Ph1 (Phase1) offset.** Additional offset for reported value. Behavior does depend on if current sharing is active or not. When no current sharing each phase get the individual offset. When current sharing active then any offset entered is shared equal between all active phases even of offset is only entered for one phase.